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EXAMINER	
LANDAU, MATTHEW C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/605,293	CHAPEK, DAVID L.	
	Examiner	Art Unit	
	Matthew C. Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-11 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-11 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 9, 10, 11, 12, and 14 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Regarding claims 9-12, the limitation “has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process” is not sufficiently supported by the originally filed application. While the specification states "plasma source ion implantation reduces the possibility of contamination of the target object by eliminating a device which employs a metal grid", at no point does the specification describe a silicon dioxide layer with a reduced amount of sputtered metal contaminants compared with a silicon dioxide layer doped using Kauffman ion implantation. Regarding claim 14, the limitation "the semiconductor substrate has reduced sputtered metal contaminants in comparison with a semiconductor substrate doped with ions deposited by a Kauffman ion implantation process” is also not sufficiently supported by the originally filed application for the same reasons presented above.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9, 10, 11, 12, and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 9-12, the limitation "has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process" renders the claim indefinite. The metes and bounds of the claim are indefinite because the ordinary artisan would not know what level of metal contaminants is required to meet the limitation. Whether or not metal contaminants are "sputtered" metal contaminants makes no structural different in the product. Further, whether or not the metal contaminants come from a Kauffman ion implantation process or another source also does not make a structural difference in the product. Considering metal contaminants can come from many different sources (including subsequent metallization processes), there is no way to determine if metal contaminants in the final product came from Kauffman ion implantation process or another source. The level of sputtered metal contaminants resulting from a Kauffman ion implantation process can vary do to varying process conditions such as implantation time and energy. The amount metal contaminants from other sources may also vary depending manufacturing techniques used to make the device. The specification provides no guidance as to the amount of metal contaminants that can be imparted when using a Kauffman ion implantation process, nor does the specification provide any guidance as to the amount of metal contaminants imparted when using the disclosed plasma source ion implantation process. Further, when looking at a final (or intermediate) product, there is no way for the ordinary artisan to determine

whether or not any metal contaminants existing in the silicon dioxide layer are from a Kauffman ion implantation process, or from another source. Therefore, the ordinary artisan would not be able to determine the level of metal contaminants covered by the scope of the claim. In view of all of the above noted considerations, the limitation does not particularly point out and distinctly claim the level of metal contaminants in the product. The above limitation if further indefinite since it is unclear if Applicant is positively reciting a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process. In other words, does the claim require two doped silicon dioxide layers? Regarding claim 14, the limitation "the semiconductor substrate has reduced sputtered metal contaminants in comparison with a semiconductor substrate doped with ions deposited by a Kauffman ion implantation process" is also not sufficiently supported by the originally filed application for the same reasons presented above.

Further regarding claim 14, the limitation "a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass" renders the claim indefinite. The listed materials are insulating materials. It is unclear how the substrate can be a semiconductor substrate when it is made of an insulating material.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 9 is rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art (hereinafter the APA).

Regarding claim 9, as best the Examiner can ascertain the claimed invention, the APA anticipates the claim. The APA discloses on page 1 lines 12-16 a semiconductor substrate, a layer of silicon dioxide on the substrate, and a layer of polycrystalline silicon formed on the silicon dioxide, the polycrystalline silicon having a smooth morphology. The APA discloses the layer of silicon dioxide having been doped with hydrogen ions. The APA is considered to inherently teach a substrate as the APA teaches DRAM's and DRAM's inherently have a substrate. Though the APA does not explicitly state a layer of polysilicon is on the silicon dioxide it is implicitly understood that the polysilicon is formed seeing that the APA discusses performing the hydrogen doping of the silicon dioxide so as to provide a thinner, smoother polysilicon film deposited on the silicon dioxide. The APA does not explicitly state the layer of silicon dioxide "has reduced sputter metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process", but this limitation is inherent. The level of metal contaminants imparted by the Kauffman ion implantation process of the APA can be considered "reduced" compared to an arbitrary ion implantation process conducted at a higher energy and/or for a longer time. Regardless of the particular parameters of the APA process, there can always be another Kauffman ion implantation process that is conductive at a higher temperature or for a longer time period. In other words, since the claim does not specify the particular conditions of the Kauffman ion implantation process, there can

always be some Kauffman ion implantation process that imparts more metal contaminants than that of the APA process.

Claims 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al. (US Pat. 5,946,585, hereinafter Zhang), as evidence by Nakanishi et al. (US Pat. 6,265,247, hereinafter Nakanishi).

Regarding claims 9 and 10, Figure 1D of Zhang discloses a semiconductor substrate (col. 4, lines 14-16); a layer of silicon dioxide 104 (col. 4, lines 48 and 49) formed on said semiconductor substrate, said silicon dioxide layer inherently containing hydrogen; and a layer of polycrystalline silicon 105 (col. 4, lines 56-58) formed on said layer of silicon dioxide, said layer of poly have a smooth morphology (at least to some degree); and a gate oxide formed on said substrate from said layer of silicon dioxide. Zhang discloses the silicon dioxide layer 104 is formed by plasma CVD (col. 4, lines 44-46). Therefore, the layer inherently contains at least some hydrogen. Nakanishi discloses that a silicon oxide film formed by plasma CVD contains hydrogen (col. 2, lines 30-34). The limitation "having been doped with hydrogen ions deposited by a plasma source ion implantation process" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966. Since no Kauffman ion implantation process is conducted during the manufacturing of the device of Zhang, it is inherent that the oxide layer has reduced sputter metal contaminants in

comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process.

Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Shufflebotham (US Pat. 5,711,998).

Regarding claim 14, as best the Examiner can ascertain the claimed invention, Figure 3 of Shufflebotham discloses a thin film transistor comprising: a semiconductor substrate 301 formed from glass (col. 5, lines 13-15), a layer of poly-Si 306A/307/306B (col. 5, lines 18-20) formed on at least a portion of said semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology (any layer can be considered smooth to at least some degree); a layer of an insulating material 308 formed on at least a portion of said layer of polycrystalline silicon; a gate oxide 308 (col. 5, lines 17 and 18) formed from said layer of insulating material; a source region and a drain region formed in said layer of polycrystalline silicon; and a gate electrode 304 formed on said insulating material. Shufflebotham discloses performing a hydrogenation process in which hydrogen ions diffuse into the poly-Si layer (see col. 6, lines 17-49, for example). In this process, it is inherent that at least some hydrogen ions reach the substrate. The limitation "implanted therein by plasma source ion implantation" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964,

966. Note that Shufflebotham does not use a Kauffman ion implantation process. Therefore, as best the Examiner can ascertain the claimed invention, it is inherent that the substrate 301 has reduced sputtered metal contaminants in comparison with a semiconductor substrate doped with ions deposited by a Kauffman ion implantation process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, Pp. 380 and 381) in view of the APA.

Regarding claim 10, Burns et al. teach a field effect transistor in figure 9.8 on page 381. Burns et al. teach a substrate, silicon dioxide layer, a layer of polycrystalline silicon over the silicon dioxide layer, and a gate oxide, a source and a drain in the substrate where a gate electrode is formed from the layer of polycrystalline silicon. Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein or the silicon dioxide layer having reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process. The APA teaches implanting hydrogen ions into silicon dioxide on page 1 lines 12-16. The APA as discussed above inherently teaches

the silicon dioxide “has reduced sputter metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process". In the combination of the references, the gate oxide would be formed from the layer of silicon dioxide having hydrogen ions implanted therein.

Burns et al. and the APA are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Burns et al. with the APA to obtain the invention of claim 10.

With regard to claim 11, Burns et al. teach on pages 380 and 381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate oxide, source, and drain formed on the substrate and a gate electrode for each transistor formed of the layer of polycrystalline silicon. The gate oxide for each transistor of the combination of references would be formed of the silicon dioxide having hydrogen atoms implanted therein.

With regard to claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs. Also, the gate

electrode is a repeating series of gate electrodes for each transistor on each die formed from the layer of polycrystalline silicon.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. Patent No. 5576229) in view of the APA.

Murata et al. teach a thin film transistor in figure 6E comprising a semiconductor substrate of glass, a layer of polycrystalline silicon 507 formed on a portion of the substrate, a insulating layer 503 formed on a portion of the polycrystalline silicon, a gate oxide, a source region 507a and drain region 507b formed in the polycrystalline silicon, and a gate electrode 504 formed on the insulating layer. Murata et al. do not teach the substrate having hydrogen ions implanted therein or the substrate oxide having reduced sputtered metal contaminants in comparison with a substrate doped with ions deposited by a Kauffman ion implantation process. The APA teaches implanting hydrogen ions into a silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. The APA as discussed above inherently teaches the silicon dioxide “has reduced sputter metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process". Murata et al. and the APA are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film.

Therefore, it would have been obvious to combine Murata et al. with the APA to obtain the invention of claim 14.

Response to Arguments

Applicant's arguments with respect to claims 9-12 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is 571-272-1731. The examiner can normally be reached on 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew C. Landau/
Primary Examiner, Art Unit 2815